REMARKS

This amendment is responsive to the Office Action dated January 26, 2006. Applicants have amended claims 50, 51, 58, 59 and 71. Claims 39-79 are pending.

Claim Objections

In the Office Action, the Examiner objected to claims 63-65 and 71 due to informalities. The Examiner was correct in assuming that claims 63-65 were meant to be left in their previously presented state. Applicants have returned claims 63-65 to their previously presented state. In addition, Applicants have amended claim 71 such that the word "aid" now reads "said." Applicants request withdrawal of the objections.

Claim Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 39-66 and 71-79 under 35 U.S.C. 102(b) as being anticipated by Hochschild et al. (USPN 5,805,589) (hereinafter "Hochschild"). Applicants respectfully traverse the rejection to the extent such rejection may be considered applicable to the amended claims. Hochschild fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(b), and provides no teaching that would have suggested the desirability of modification to include such features.

Claims 39-49

Hochschild fails to teach or suggest an apparatus that includes a set of input ports, a FIFO (first in, first out) storage buffer, and request logic coupling said set of input ports to said FIFO storage buffer, wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports, as required by Applicants' independent claims 39 and 46.

The Examiner stated that Hochschild discloses an input LRU (least recently used) arbiter 385 in the switching circuit 25 that anticipates the request logic described in Applicants' claims 39 and 46 as coupling a set of input ports to the FIFO storage buffer and simultaneously writing data to the FIFO storage buffer for at least two of the input ports. The Examiner stated that the input LRU arbiter 385 receives input request signals from the input ports 310 and issues a write enable signal to the central queue 350 so that 64-bit incoming data chunks are written to chunk

storage RAM 715 within the central queue 350. However, unlike the request logic of Applicants' invention, the input LRU arbiter 385 described by the Hochschild reference does not simultaneously write data to the central queue 350 for at least two of the input ports 310.

The only use of the term "simultaneously" in the detailed description of Hochschild appears at col. 22, ln. 32 and ln. 34, where Hochschild refers to transmitters simultaneously making requests to *read* data from central queue 350. Hochschild characterizes the output contention as simultaneous "read (output) access," and provides the example of two or more transmitters simultaneously requesting service. Thus, Hochschild is referring to attempted simultaneous *reads* from a central queue, and not to a FIFO that supports simultaneous *writes* to the FIFO from different input ports, as required by claim 1.

Second, Hochschild makes clear that even simultaneous reads are **not** supported. Hochschild states that only "[i]f contention does ***not*** exist ... LRU arbiter 368 issues a grant signal and applies that signal to leads 647."

Third, with respect to FIG. 8 cited by the Examiner, Hochschild discloses that the central queue 350 includes a chunk storage RAM 715 that stores "message chunks" received from input ports 310 of the switching circuit 25.[1] Earlier in the disclosure, Hochschild makes clear that message chunks are **not** supplied to and written from the central queue 350 simultaneous, but rather on a **time-multiplexed basis**.[2] Each input port 310 supplies its associated message chunk to the central queue 350 during a different, corresponding clock cycle and each output port 380 obtaining a message chunk destined therefore from the central queue 350 during its associated corresponding clock cycle.[3] In this manner, both reads and writes to the central queue are sequential and non-overlapping, and cannot be considered to be simultaneous for at least two different input ports.

In other words, Hochschild teaches a storage buffer that receives data from each of the input ports 310 during a corresponding clock cycle such that the storage buffer can **never** receive data from more than one of the input ports 310 during the **same** clock cycle. Therefore, the input LRU arbiter 385 disclosed by the Hochschild reference cannot **simultaneously** write data to the storage buffer for at least two of the input ports 310. Clearly, writing chunks (i.e., large blocks)

[1] *Hochschild et al.*, Col. 24, lines 40-43.
[2] *Hochschild et al.*, Col. 12, lines 26-44.
[3] *Hochschild et al.*, Col. 12, lines 26-44.

of data for a single input port 310 at a time, as described by Hochschild, fails to teach or suggest request logic that **simultaneously** writes data to the FIFO storage buffer **for at least two** of the input ports, as required by Applicants' claims 39 and 46.

For at least the reasons described above in reference to Applicants' independent claims 39 and 46, Applicants' dependent claims 40-45 and 47-49 are also in condition for allowance.

Claims 50-66

Hochschild fails to teach or suggest a sink port within a cross-bar switch that includes a multiple entry point FIFO (first in, first out) having a plurality of data inputs in communication with a set of input ports to simultaneously accept and store data for at least two of the input ports, as required by Applicants' independent claims 50 and 58 as amended.

The Examiner stated that Hochschild discloses a switching circuit 25 including a central queue 350 that anticipates the multiple entry point FIFO described in Applicants' amended claims 50 and 58. Contrary to the Examiner's assertion, the central queue 350 taught by the Hochschild reference does not comprise a multiple entry point FIFO capable of simultaneously accepting and storing data for at least two of the input ports. As described above, Hochschild states that message chunks are supplied to and written from the central queue 350 on a time-multiplexed basis, with each input port 310 supplying its associated message chunk to the central queue 350 during a different, corresponding clock cycle and each output port 380 obtaining a message chunk destined therefore from the central queue 350 during its associated corresponding clock cycle. Therefore, the central queue 350 can never receive and store data from more than one of the input ports 310 during the same clock cycle. Clearly, Hochschild fails to describe a multiple entry point FIFO that simultaneously accepts and stores data for at least two of the input ports, as required by Applicants' amended claims 50 and 58.

In a similar manner, the Hochschild reference fails to teach or suggest each and every feature of Applicants' dependent claims 51-57 and 59-66. For example, claims 51 and 59, as amended, recite the multiple entry point FIFO including a FIFO storage buffer, and request logic coupling the set of input ports to the FIFO storage buffer, wherein the request logic simultaneously writes data to the FIFO storage buffer for at least two of the input ports.

Unlike Applicants' claimed invention, Hochschild teaches a storage buffer that receives data from input ports in a particular order and outputs data to output ports based on a classification assigned to the data, and <u>not</u> based on the particular order in which the data was received from the input ports. Hochschild fails to describe FIFO storage buffer, as required by Applicants' claims 51 and 59. In addition, Hochschild teaches a storage buffer that receives data from each of the input ports 310 during a corresponding clock cycle such that the storage buffer can <u>never</u> receive data from more than one of the input ports 310 during the same clock cycle. Therefore, Hochschild fails to describe request logic that simultaneously writes data to the FIFO storage buffer for at least two of the input ports, as required by Applicants' claims 51 and 59.

For at least the reasons described above in reference to Applicants' independent claims 50 and 58, Applicants' other dependent claims 52-57 and 60-70 are also in condition for allowance.

Claims 71-79

Hochschild fails to teach or suggest a method for a sink port in a cross-bar switch to collect data in a FIFO comprising accepting data from a second data packet at <u>substantially the same time</u> as accepting data from a first data packet, and storing the data from the second data packet in the FIFO <u>at substantially the same time</u> as storing the data from the first data packet in the FIFO, as required by Applicants' independent claim 71 as amended.

The Examiner stated that Hochschild discloses chunks of data received from input ports 310 in the switching circuit 25 and stored in chunk storage RAM 715 in the central queue 350 that anticipate accepting and storing data from a first data packet and data from a second data packet. However, unlike Applicants' claimed invention, Hochschild does not describe accepting and storing data from a second data packet <u>at substantially the same time</u> as accepting and storing data from a first data packet.

Hochschild discloses that the central queue 350 includes a chunk storage RAM 715 that stores message chunks received from input ports 310 of the switching circuit 25. Hochschild also states that message chunks are supplied to and written from the central queue 350 on a time-multiplexed basis, with each input port 310 supplying its associated message chunk to the central queue 350 during a corresponding clock cycle and each output port 380 obtaining a message

chunk destined therefore from the central queue 350 during its associated corresponding clock cycle.

In other words, Hochschild teaches a storage buffer that receives a subset of a data packet from each of the input ports 310 during a corresponding clock cycle such that the storage buffer can never accept and store data from more than one data packet during the same clock cycle. Therefore, Hochschild fails to describe accepting and storing data from a second data packet at substantially the same time as accepting and storing data from a first data packet, as required by Applicants' amended claim 71.

For at least the reasons described above in reference to Applicants' independent claim 71, Applicants' dependent claims 72-79 are also in condition for allowance.

Hochschild fails to disclose each and every limitation set forth in claims 39-66 and 71-79. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicants' claims 39-66 and 71-79 under 35 U.S.C. 102(b). Withdrawal of this rejection is requested.

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 67-70 under 35 U.S.C. 103(a) as being unpatentable over Hochschild in view of Dai et al. (USPN 6,658,016) (hereinafter "Dai"). Applicants respectfully traverse the rejection. The applied references fail to disclose or suggest the inventions defined by Applicants' claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

Hochschild and Dai, either separately or in combination, lack any teaching that would have suggested a cross-bar switch having set of data rings in communication with a set of input ports and a set of sink ports of that cross-bar switch. As described above, Hochschild fails to teach a cross-bar switch including a sink port with a multiple entry point FIFO having a plurality of data inputs in communication with a set of input ports to simultaneously accept and store data for at least two of the input ports, as recited by Applicants' independent claim 58 from which claims 67-70 depend. The Dai reference provides no teaching capable of overcoming the deficiencies of Hochschild.

The Examiner correctly acknowledged that Hochschild fails to disclose a cross-bar switch having a set of data rings in communication with a set of input ports and a set of sink ports of that cross-bar switch. However, the Examiner asserted that Dai discloses this feature. On the contrary, Dai fails to describe a cross-bar switch having a set of data rings in communication with a set of input ports and a set of sink ports <u>within</u> the cross-bar switch. Instead, Dai describes a packet switching fabric in which a plurality of switching devices are coupled in a ring fashion. The Dai switch fabric is properly viewed as a ring of switches. For example, FIG. 1 of Dai illustrates four distinct switching devices 12 coupled in a ring-like manner using an external data ring 18 and a control ring 24. The data ring 18 includes a plurality of data ring segments each coupling a corresponding adjacent pair of the devices together to ultimately form a ring.

In contrast, Applicants describe and claim a single cross-bar switch in which the cross-bar switch itself includes data rings for transferring packets directly between the input ports and the output (sink) ports of that same cross-bar switch. For purposes of clarity, Applicants refer the Examiner to Figure 2 of the present application that illustrates an exemplary internal architecture of Applicants' described cross-bar switch. When properly viewed, the Dai switches that may be connected to form a "ring" are fundamentally different from the internal apparatus architecture described and claimed by the Applicants. Dai fails to teach or suggest that the internal architecture of any of the switches comprises a ring topology that connects the input ports and the output ports within the individual switch. Thus, the Examiner is incorrect when asserting that Dai teaches a cross-bar switch comprising a set of input ports, a set of sink ports in communication with the set of input ports, and a set of data rings in communication with the set of input ports and the set of sink ports.

For at least these reasons, the Examiner has failed to establish a prima facie case for non-patentability of Applicants' claims 67-70 under 35 U.S.C. 103(a). Withdrawal of this rejection is requested.

CONCLUSION

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Date: April 26, 2006

SHUMAKER & SIEFFERT, P.A.
8425 Seasons Parkway, Suite 105
St. Paul, Minnesota 55125
Telephone: 651.735.1100
Facsimile: 651.735.1102

By: Kent J. Sieffert

Name: Kent J. Sieffert
Reg. No.: 41,312